IN THE CLAIMS

Please cancel claims 4, 5 and 9, and amend claim 1, all without prejudice as follows.

1 (currently amended): A method of designing a clock tree in an integrated circuit, comprising the steps of:

collecting a set of sink locations in a master list and a set of blocked areas;

(a) selecting a temporary insertion point (TIP);

(b) enclosing ~~the~~ a sink at ~~the~~ a first level ~~furthest~~ farthest from the TIP in a bin that includes a first subset of sinks and remove the first subset of sinks from the master list;

(c) assigning a first-level structured clock buffer (SCB) to the bin, in which said step (c) of assigning a first-level SCB to the bin comprises the steps of attempting to place a horizontal SCB, then attempting to place a vertical SCB in a central location when a horizontal SCB will not fit in said central location;

repeating steps (a), (b) and (c) above for the remaining sinks in the first level of buffers and subsequent levels until a root level is reached;

improving the symmetry of the tree by moving the SCB locations within constraints to concentrate SCBs in rows and columns;

connecting the root level TIP to lower levels; and

connecting a source (S) of clock signals to the root level TIP.

2-10 (canceled)